#### HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

- 500-mA Rated Collector Current (Single Output)
- High-Voltage Outputs . . . 100 V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
- Relay Driver Applications
- Higher-Voltage Versions of ULN2003A and ULN2004A, for Commercial Temperature Range

#### SN75468 . . . D, N, OR NS PACKAGE SN75469 . . . D OR N PACKAGE (TOP VIEW) 1B 16 T 1C 2B [ 15 **1** 2C 2 3В П 14**∏** 3C 48 ∏ 13 **∏** 4C 5В П 5 12 \ 5C 6B [ 6 11 1 6C 7B [ 10 7C 9 T COM Ε 8

#### description/ordering information

The SN75468 and SN75469 are high-voltage, high-current Darlington transistor arrays. Each consists of seven npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of each Darlington pair is 500 mA. The Darlington pairs may be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers.

The SN75468 has a 2700- $\Omega$  series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS. The SN75469 has a 10.5-k $\Omega$  series base resistor to allow its operation directly with CMOS or PMOS that use supply voltages of 6 to 15 V. The required input current is below that of the SN75468.

#### ORDERING INFORMATION

TA	PACKAGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
	PDIP (N)	Tube of 25	SN75468N	SN75468N
0°C to 70°C	2010 (D)	Tube of 40	SN75468D	ON 75 400
	SOIC (D)	Reel of 2500	SN75468DR	SN75468
	SOP (NS)	Reel of 2000	SN75468NSR	SN75468
	PDIP (N)	Tube of 25	SN75469N	SN75469N
	SOIC (D)	Tube of 40	SN75469D	SN75469
	3010 (0)	Reel of 2500	SN75469DR	3117 3403

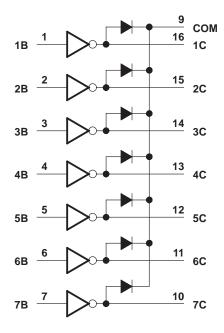
<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



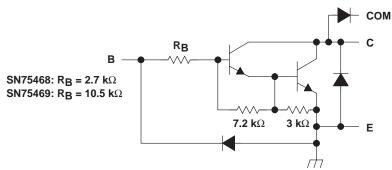
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#### logic diagram



### schematic (each Darlington pair)



All resistor values shown are nominal.

### SN75468, SN75469 DARLINGTON TRANSISTOR ARRAYS

SLRS023D - DECEMBER 1976 - REVISED NOVEMBER 2004

### absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)†

Collector-emitter voltage, V <sub>CE</sub>		100 V
Input voltage, V <sub>I</sub> (see Note 1)		
Peak collector current (see Figures 14 and 15)		500 mA
Output clamp current, I <sub>OK</sub>		500 mA
Total emitter-terminal current		–2.5 A
Package thermal impedance, θ <sub>JA</sub> (see Notes 2 and 3):	: D package	73°C/W
	N package	67°C/W
	NS package	64°C/W
Operating virtual junction temperature, T <sub>J</sub>		150°C
Storage temperature range, T <sub>stg</sub>		$-65^{\circ}\text{C}$ to $150^{\circ}\text{C}$

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.
  - 2. Maximum power dissipation is a function of  $T_J(max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(max) T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.



## SN75468, SN75469 DARLINGTON TRANSISTOR ARRAYS

SLRS023D - DECEMBER 1976 - REVISED NOVEMBER 2004

# electrical characteristics, $T_A = 25^{\circ}C$ (unless otherwise noted)

PARAMETER		TEST TEST CONDITIONS		NDITIONS	SN75468			SN75469			UNIT
		FIGURE	TEST CO	TEST CONDITIONS		TYP	MAX	MIN	TYP	MAX	UNIT
				I <sub>C</sub> = 125 mA						5	
				$I_C = 200 \text{ mA}$			2.4			6	
V		5	V 0.V	$I_C = 250 \text{ mA}$			2.7				V
V <sub>I(on)</sub>	On-state input voltage	5	V <sub>CE</sub> = 2 V	$I_C = 275 \text{ mA}$						7	
				$I_C = 300 \text{ mA}$			3				
				$I_C = 350 \text{ mA}$						8	
	Collector-emitter saturation voltage		$I_I = 250 \mu A$ ,	$I_C = 100 \text{ mA}$		0.9	1.1		0.9	1.1	V
VCE(sat)		6	$I_I = 350 \mu A$ ,	$I_C = 200 \text{ mA}$		1	1.3		1	1.3	
, ,			$I_{I} = 500 \mu A$ ,	$I_C = 350 \text{ mA}$		1.2	1.6		1.2	1.6	
VF	Clamp-diode forward voltage	8	IF = 350 mA			1.7	2		1.7	2	V
	Collector cutoff current	1	V <sub>CE</sub> = 100 V,	I <sub>I</sub> = 0			50			50	
ICEX			V <sub>CE</sub> = 100 V,	I <sub>I</sub> = 0			100			100	μΑ
		2	T <sub>A</sub> = 70°C	V <sub>I</sub> = 1 V						500	
I <sub>I(off)</sub>	Off-state input current	3	V <sub>CE</sub> = 50 V, T <sub>A</sub> = 70°C	$I_{C} = 500 \mu A,$	50	65		50	65		μΑ
	Input current		V <sub>I</sub> = 3.85 V			0.93	1.35				
lį		4	V <sub>I</sub> = 5 V						0.35	0.5	mA
			V <sub>I</sub> = 12 V						1	1.45	
	Clamp-diode reverse	_	V <sub>R</sub> = 100 V				50			50	
IR	current	7	$V_R = 100 V$ ,	T <sub>A</sub> = 70°C			100			100	μΑ
Ci	Input capacitance		$V_{I} = 0$ ,	f = 1 MHz		15	25		15	25	pF

# switching characteristics, $T_A = 25^{\circ}C$ free-air temperature

	PARAMETER	Т	EST CONDITIC	MIN	TYP	MAX	UNIT	
tPLH	Propagation delay time, low-to-high-level output	V <sub>S</sub> = 50 V,	R <sub>L</sub> = 163 Ω,	C <sub>L</sub> = 15 pF,		0.25	1	μs
<sup>t</sup> PHL	Propagation delay time, high-to-low-level output	See Figure 9				0.25	1	μs
Vон	High-level output voltage after switching	$V_S = 50 V$ ,	I <sub>O</sub> ≈ 300 mA,	See Figure 10	V <sub>S</sub> - 20			mV

### PARAMETER MEASUREMENT INFORMATION

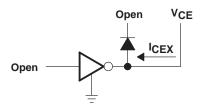


Figure 1. I<sub>CEX</sub>

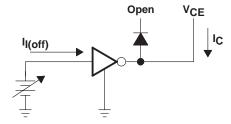


Figure 3. I<sub>I(off)</sub>

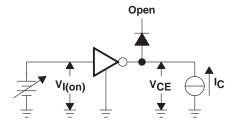


Figure 5. V<sub>I(on)</sub>

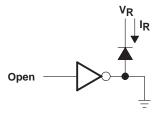


Figure 7. I<sub>R</sub>

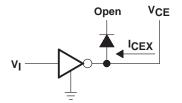


Figure 2. I<sub>CEX</sub>

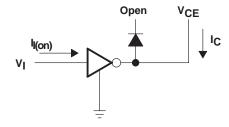
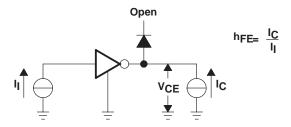


Figure 4. I<sub>I</sub>



NOTE: I<sub>I</sub> is fixed for measuring V<sub>CE(sat)</sub>, variable for measuring h<sub>FE</sub>.

Figure 6. hFE, VCE(sat)

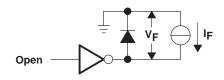


Figure 8. V<sub>F</sub>

#### PARAMETER MEASUREMENT INFORMATION

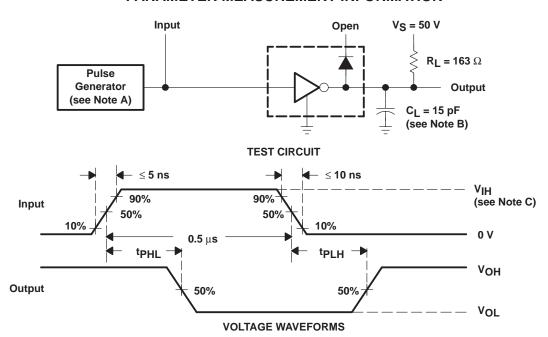


Figure 9. Test Circuit and Voltage Waveforms

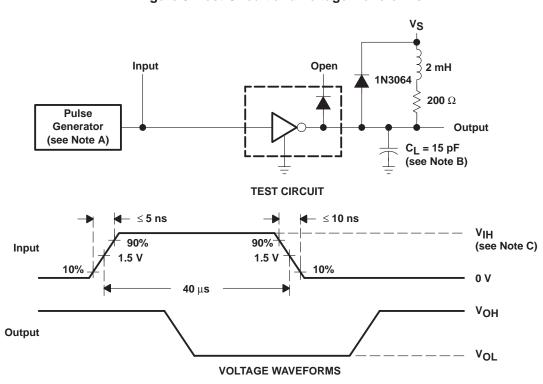


Figure 10. Latch-Up Test Circuit and Voltage Waveforms

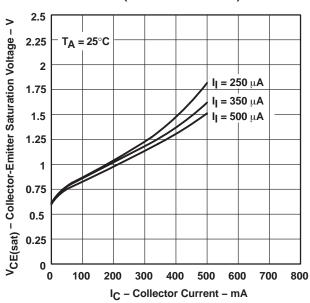
NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz,  $Z_O = 50 \Omega$ .

- B. C<sub>L</sub> includes probe and jig capacitance.
- C. For testing the '468,  $V_{IH} = 3 \text{ V}$ ; for the '469,  $V_{IH} = 8 \text{ V}$ .



#### **TYPICAL CHARACTERISTICS**

COLLECTOR-EMITTER
SATURATION VOLTAGE
vs
COLLECTOR CURRENT
(ONE DARLINGTON)



COLLECTOR-EMITTER
SATURATION VOLTAGE
vs
COLLECTOR CURRENT
(TWO DARLINGTONS PARALLELED)

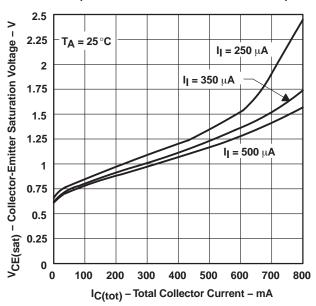


Figure 11 Figure 12

#### **COLLECTOR CURRENT**

VS **INPUT CURRENT** 500  $R_L = 10 \Omega$ 450 T<sub>A</sub> = 25 °C - Collector Current - mA 400  $V_S = 10 V$ 350 Vs = 8 V 300 250 200 150 100 50 0 0 25 50 75 100 125 150 175 200 I<sub>I</sub> - Input Current - mA



#### THERMAL INFORMATION

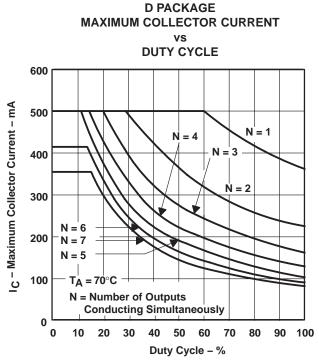


Figure 14

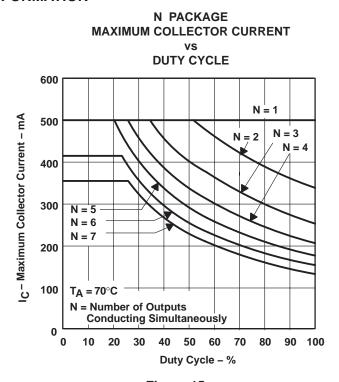


Figure 15

#### **APPLICATION INFORMATION**

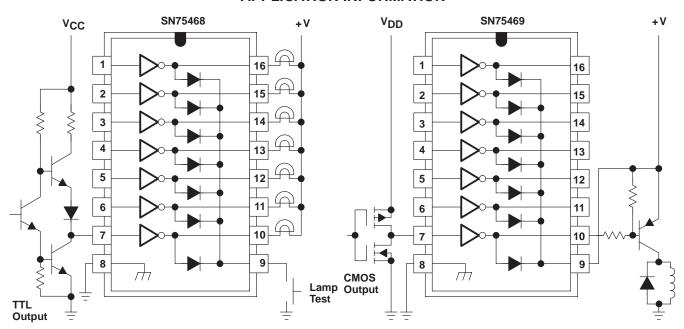


Figure 16. TTL to Load

Figure 17. Buffer for Higher Current Loads

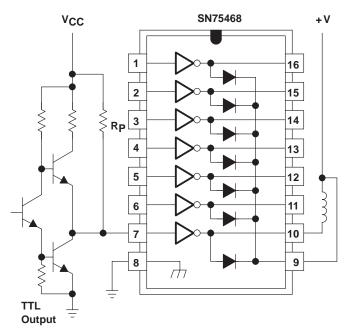


Figure 18. Use of Pullup Resistors to Increase Drive Current





30-Mar-2005

#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN75468D	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN75468DR	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN75468N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN75468NSR	ACTIVE	SO	NS	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN75469D	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN75469DR	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN75469N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## N (R-PDIP-T\*\*)

### PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



# D (R-PDSO-G16)

### PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012 variation AC.



#### **MECHANICAL DATA**

### NS (R-PDSO-G\*\*)

## 14-PINS SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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